## IN THE CLAIMS

1.- 8. (Canceled)

9. - 27. (Withdrawn)

28. - 35. (Canceled)

36. - 45. (Withdrawn)

46. - 51. (Canceled)

52. - 58. (Withdrawn)

~~59~~. (Amended) An electronic system, comprising:

a processor; and

a memory device coupled to processor, wherein the memory device includes a programmable decoder comprising:

a number of address lines;

a number of output lines;

wherein the address lines, and the output lines form an array;

a number of logic cells formed at the intersections of output lines and address lines, wherein each of the logic cells includes a vertical non-volatile memory cell including:

a vertical pillar extending outwardly from a semiconductor substrate at intersections of the input lines and interconnect lines and at the intersections of the interconnect lines and the output lines, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

a number of control gates opposing the floating gates, wherein the number of control gates are separated

from the number of floating gates by a low tunnel barrier [integrate] intergate insulator;

a number of buried source lines formed of single crystalline semiconductor material and disposed below the pillars in the array for interconnecting with the first source/drain regions of column adjacent pillars in the array.

60. (Original) The electronic system of claim 59, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of PbO, $Al_2O_3$, $Ta_2O_5$, $TiO_2$, $ZrO_2$, and $Nb_2O_5$.

61. (Original) The electronic system of claim 59, wherein each floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

62. (Original) The electronic system of claim 61, wherein each control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

63. (Original) The electronic system of claim 59, wherein each floating gate is a vertical floating gate formed in a trench below a top surface of each pillar such that each trench houses a pair of floating gates opposing the body regions in adjacent pillars on opposing sides of the trench.

64. (Original) The electronic system of claim 63, wherein the number of control gates are formed in the trench below the top surface of the pillar and between the pair of floating gates, wherein each pair of floating gates shares a single control gate, and wherein each floating gate includes a vertically oriented floating gate having a vertical length of less than 100 nanometers.

65. (Original) The electronic system of claim 63, wherein the number of control gates are formed in the trench below the top surface of the pillar and between the pair of floating gates such that each trench houses a pair of control gate lines each addressing the floating gates one on

opposing sides of the trench respectively, and wherein the pair of control gate lines are separated by an insulator layer.

8 5
~~66.~~ (Original) The electronic system of claim ~~65~~, wherein the number of control gates are disposed vertically above the floating gates, and wherein each pair of floating gates shares a single control gate.

Could A7

9 5
~~67.~~ (Original) The electronic system of claim ~~65~~, wherein the number of control gates are disposed vertically above the floating gates, and wherein each one of the pair of floating gates is addressed by an independent one of the number of control gates.

10 1
~~68.~~ (Original) The electronic system of claim ~~59~~, wherein each floating gate is a horizontally oriented floating gate formed in a trench below a top surface of each pillar such that each trench houses a floating gate opposing the body regions in adjacent pillars on opposing sides of the trench, and wherein each horizontally oriented floating gate has a vertical length of less than 100 nanometers opposing the body region of the pillars.

11 10
~~69.~~ (Original) The electronic system of claim ~~68~~, wherein the number of control gates are disposed vertically above the floating gates.

70. - 76. (Canceled)

12
~~77.~~ (Amended) A method for forming an in service programmable logic array, comprising:

forming a plurality of address lines;

A3 forming a plurality of output lines, wherein the plurality of output and address lines form an array; and

forming a number of logic cells at the intersections of the output and address lines, wherein forming a number of logic cells includes forming a number of vertical non-volatile memory cells including:

forming a vertical pillar extending outwardly from a semiconductor substrate at intersections of the input lines and interconnect lines

A

and at the intersections of the interconnect lines and the output lines, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

forming a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

forming a number of control gates opposing the floating gates; and

forming a low tunnel barrier intergate insulator to separate the control gate from the floating gate; and

forming a number of buried source lines formed of single crystalline semiconductor material and disposed below the pillars in the array for interconnecting with the first source/drain regions of column adjacent pillars in the array.

a3

13 12
~~78~~. (Original) The method of claim ~~77~~, wherein forming the low tunnel barrier intergate insulator includes forming a metal oxide insulator selected from the group consisting of PbO, $Al_2O_3$, $Ta_2O_5$, $TiO_2$, $ZrO_2$, and $Nb_2O_5$.

14 12
~~79~~. (Original) The method of claim ~~77~~, wherein forming each floating gate includes forming a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

15 12
~~80~~. (Original) The method of claim ~~77~~, wherein forming each control gate includes forming a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

16 12
~~81~~. (Original) The method of claim ~~77~~, wherein forming each floating gate includes forming a vertical floating gate formed in a trench below a top surface of each pillar such that each trench houses a pair of floating gates opposing the body regions in adjacent pillars on opposing sides of the trench.

17 16
~~82~~. (Original) The method of claim ~~81~~, wherein forming the number of control gates includes forming the control gates in the trench below the top surface of the pillar and between

A

the pair of floating gates, wherein each pair of floating gates shares a single control gate line, and wherein each floating gate includes a vertically oriented floating gate having a vertical length of less than 100 nanometers.

18 16
~~83~~. (Original) The method of claim ~~81~~, wherein forming the number of control gates includes forming the control gates in the trench below the top surface of the pillar and between the pair of floating gates such that each trench houses a pair of control gates each addressing the floating gates one on opposing sides of the trench respectively, and wherein the pair of control gates are separated by an insulator layer.

Canceled A3

19 16
~~84~~. (Original) The method of claim ~~81~~, wherein forming the number of control gates includes forming the control gates disposed vertically above the floating gates, and wherein each pair of floating gates shares a single control gate.

20 16
~~85~~. (Original) The method of claim ~~81~~, wherein forming the number of control gates includes forming the control gates disposed vertically above the floating gates, and wherein each one of the pair of floating gates is addressed by an independent one of the number of control gates.

21 12
~~86~~. (Original) The method of claim ~~77~~, wherein forming each floating gate includes forming a horizontally oriented floating gate formed in a trench below a top surface of each pillar such that each trench houses a floating gate opposing the body regions in adjacent pillars on opposing sides of the trench, and wherein each horizontally oriented floating gate has a vertical length of less than 100 nanometers opposing the body region of the pillars.

22 21
~~87~~. (Original) The method of claim ~~86~~, wherein forming the number of control gates includes forming the control gates disposed vertically above the floating gates.

88. - 98. (Canceled)

A

B 89. (New) An electronic system, comprising:

a processor; and

a memory device coupled to processor, wherein the memory device includes a programmable decoder comprising:

A4

a number of address lines;

a number of output lines;

wherein the address lines, and the output lines form an array;

a number of logic cells formed at the intersections of output lines and address lines, wherein a logic cell includes a vertical non-volatile memory cell including:

a vertical pillar extending outwardly from a semiconductor substrate at intersections of the input lines and interconnect lines and at the intersections of the interconnect lines and the output lines, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide, wherein the floating gates include a polysilicon layer and a metal layer;

a number of control gates opposing the floating gates, wherein the number of control gates are separated from the number of floating gates by a low tunnel barrier, metal oxide intergate insulator, wherein the intergate insulator contacts the metal layer of the floating gate;

a number of buried source lines formed of single crystalline semiconductor material and disposed below the pillars in the array for interconnecting with the first source/drain regions of column adjacent pillars in the array.

A

~~100~~. (New) The electronic system of claim ~~99~~, wherein the low tunnel barrier, metal oxide intergate insulator includes a metal oxide insulator selected from the group consisting of PbO, $Al_2O_3$, $Ta_2O_5$, $TiO_2$, $ZrO_2$, and $Nb_2O_5$.

~~101~~. (New) The electronic system of claim ~~99~~, wherein each control gate includes a polysilicon layer and a metal layer, the metal layer being in contact with the low tunnel barrier, metal oxide intergate insulator.

~~102~~. (New) An electronic system, comprising:

a processor; and

a memory device coupled to processor, wherein the memory device includes a programmable decoder comprising:

a number of address lines;

a number of output lines;

wherein the address lines, and the output lines form an array;

a number of logic cells formed at the intersections of output lines and address lines, wherein a logic cell includes a vertical non-volatile memory cell including:

a vertical pillar extending outwardly from a semiconductor substrate at intersections of the input lines and interconnect lines and at the intersections of the interconnect lines and the output lines, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide, wherein one floating gate includes a vertically oriented floating gate having a vertical length of less than 100 nanometers;

a number of control gates opposing the floating gates, wherein the number of control gates are separated from the number of floating gates by a low tunnel barrier intergate insulator;

a number of buried source lines formed of single crystalline semiconductor material and disposed below the pillars in the array for interconnecting with the first source/drain regions of column adjacent pillars in the array.

103. (New) The electronic system of claim 102, wherein each of the floating gates includes a vertically oriented floating gate having a vertical length of less than 100 nanometers.

104. (New) The electronic system of claim 102, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of PbO, $Al_2O_3$, $Ta_2O_5$, $TiO_2$, $ZrO_2$, and $Nb_2O_5$.

105. (New) A method for forming an in service programmable logic array, comprising:

forming a plurality of address lines;

forming a plurality of output lines, wherein the plurality of output and address lines form an array; and

forming a number of logic cells at the intersections of the output and address lines, wherein forming a number of logic cells includes forming a number of vertical non-volatile memory cells including:

forming a vertical pillar extending outwardly from a semiconductor substrate at intersections of the input lines and interconnect lines and at the intersections of the interconnect lines and the output lines, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

forming a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide, wherein forming the number of floating gates includes forming a polysilicon layer and a metal layer;

forming a number of control gates opposing the floating gates; and

forming a low tunnel barrier intergate insulator to separate the control gate from the floating gate and to contact the metal layer of the number of floating gates;

forming a number of buried source lines formed of single crystalline semiconductor material and disposed below the pillars in the array for interconnecting with the first source/drain regions of column adjacent pillars in the array.

~~106~~. (New) The method of claim ~~105~~, wherein forming the low tunnel barrier intergate insulator includes forming a metal oxide insulator selected from the group consisting of PbO, $Al_2O_3$, $Ta_2O_5$, $TiO_2$, $ZrO_2$, and $Nb_2O_5$.

~~107~~. (New) The method of claim ~~105~~, wherein forming the number of floating gates includes forming a vertically oriented floating gate having a dimension of less than 100 nanometers.